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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/539,224	06/16/2005	Vincent Charles Venezia	BE02 0043 US1	4536

65913 7590 04/08/2008

NXP, B.V.
NXP INTELLECTUAL PROPERTY DEPARTMENT
M/S41-SJ
1109 MCKAY DRIVE
SAN JOSE, CA 95131

EXAMINER	
SINGAL, ANKUSH K	

ART UNIT	PAPER NUMBER
2823	

NOTIFICATION DATE	DELIVERY MODE
04/08/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/539,224	VENEZIA ET AL.	
	Examiner	Art Unit	
	ANKUSH k. SINGAL	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 February 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on February 04,2008 has been entered.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1,2 and 10 are rejected under 35 U.S.C. 102(b) as being anticipated by Wang et al.(US 6,074,922).

Re. claim 1, Wang et al. discloses a method of manufacturing a semiconductor device with a semiconductor body of a semiconductor material, the semiconductor device including field effect transistor having a source and drain region at a surface of the semiconductor body, and having a gate region between the source and drain region , the gate region including a semiconductor region of a further semiconductor material

that is separated from the surface of the semiconductor body by a gate dielectric, the method comprising: forming a gate dielectric (14) on the surface of the semiconductor substrate(same as semiconductor body)(10); forming a semiconductor region (16) on the gate dielectric (14); depositing a sacrificial region(30) on top of the semiconductor region(16); after depositing the sacrificial region(30), forming spacers(34) adjacent to the gate region for forming the source and drain regions; forming the source and drain regions(36) on the surface of the semiconductor body ; after forming the source and drain regions, selectively etching the sacrificial region(30) with respect to the semiconductor region; depositing a metal layer (40) on the source region, drain region, and the gate region(Figure 6); forming a compound(42) of the metal layer and the semiconductor material; and forming a compound that includes at least a substantial portion of the gate region, of the metal layer and further semiconductor material(Figure 8).

Re. claim 2, Wang et al. discloses having the sidewall spacers(same as spacers)(34) formed by depositing a layer of dielectric material on top of the substrate on which the gate region comprising the conductive layer(16) and the dielectric layer(same as sacrificial region) (30) is present and by subsequently removing the deposited layer on top of and on both sides of the gate region by etching (Column 3,line 53-57).

Re. claim 10, Wang et al. discloses a semiconductor device comprising a field effect transistor obtained by a method as claimed in any of the preceding claims.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 3-7 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wang et al.(US 6,074,922) in view of Hashimoto(US 2001/0003056).

Re. claim 3, Wang et al. discloses all the limitations except having the semiconductor region completely consumed during the formation of the compound of the metal and the further semiconductor material.

However, Hashimoto discloses having gate electrode(120)(same as semiconductor region) completely consumed during the formation of the CoSi.sub.2 layer(same as compound)of the metal layer and the further semiconductor material(Para[0096],line 1-2).

It would have been obvious for one with ordinary skill in the art at the time the invention was made to modify Wang et al. as taught by Hashimoto to have the semiconductor region completely consumed during the formation of the compound of the metal and the further semiconductor material to minimizes the wiring resistance of the gate electrode (Para[0094],line 4-5).

Re. claim 4, Wang et al. discloses all the limitations except the limitations disclosed in claim 4. However, Hashimoto teaches the formation of the CoSi.sub.2 layer(same as compound) between the metal and the semiconductor material and the metal and the

further semiconductor material is carried out in two separate heating steps, the first heating step resulting in an intermediate compound with a low content of the semiconductor material or of the further semiconductor material and in the second heating step the intermediate compound being converted to the compound having a higher content of the semiconductor material or of the further semiconductor material(Para[0096]).

It would have been obvious for one with ordinary skill in the art at the time the invention was made to modify Wang et al. as taught by Hashimoto to have the formation of compound with two step heating to have he surface portion of the Co.sub.2Si layer or CoSi layer prevented from being exposed during the high-temperature reaction and is therefore silicon-rich so that the surface energy of the Co.sub.2Si layer or CoSi layer is lower than in the conventional embodiment. As a result, agglomeration is less likely to occur at the surface of the Co.sub.2Si layer or CoSi layer so that a gate electrode composed of the CoSi.sub.2 layer with good uniformity in reaction thickness is formed(Para [0097].

Re. claims 5, Wang et al. discloses all the limitations except the limitations disclosed in claim 5.

However, Hashimoto teaches that between the two heating steps, a part of the cobalt film (same as metal layer) which has not reacted to form the intermediate compound is removed by etching (Para [0073],line 6-9).

It would have been obvious for one with ordinary skill in the art at the time the invention was made to modify Wang et al. as taught by Hashimoto to have cobalt film (same as metal layer) which has not reacted to form the intermediate compound is removed by etching so that agglomeration is less likely to occur at the surface of the Co.sub.2Si layer or CoSi layer so that a gate electrode composed of the CoSi.sub.2 layer with good uniformity in reaction thickness is formed([Para[0097]).

Re. claim 6, Wang et al. discloses all the limitations except the limitations disclosed in claim 6.

However, Hashimoto teaches having a silicon film(same as layer)of the further semiconductor material is deposited on the surface of the gate electrode(same as semiconductor body).

It would have been obvious for one with ordinary skill in the art at the time the invention was made to modify Wang et al. as taught by Hashimoto to have a layer deposited on

the surface of the gate electrode to minimizes the wiring resistance of the gate electrode (Para[0094],line 4-5).

Re. claim 7, Wang et al. discloses all the limitations except the limitations disclosed in claim 7. However, Hashimoto teaches that after the second heating step, a part of the silicon film(same as layer)of the further semiconductor material which has not reacted to form the compound is removed by etching(Para[0080],line1-3).

It would have been obvious for one with ordinary skill in the art at the time the invention was made to modify Wang et al. as taught by Hashimoto a part of the silicon film(same as layer)of the further semiconductor material which has not reacted to form the compound is removed by etching to achieve a higher speed operation and low power consumption(Para[0089],line 15-16).

Re. claim 9 as discussed above in claim 4, Wang et al. and Hashimoto discloses semiconductor material chosen is silicon (column 3,line 11-13), and for the metal silicide layer(same as compound)(42) for the compound of the metal and the semiconductor material and the further semiconductor material a metal silicide is chosen(column 4,line 1-8, Wang et al.).

Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wang et al.(US 6,074,922) in view of Wu(US 6,348,390).

Re. claim 8 as discussed above in claim 1, Wang et al. discloses all the limitations as discussed above in claim 1 except after the formation of the compounds of the metal and the semiconductor material and of the metal and the further semiconductor material, the spacers are removed.

However, Wu discloses after the formation of the metal silicide layer(same as compound)(28) of the metal and semiconductor material(column 5,line 54-58), the spacers(22) are removed(Column 6,line 1-2).

Therefore it would have been obvious for one with ordinary skill in the art at the time the invention was made to provide Wang et al. structure with method of removing spacer of Wu et al. to form extended source/drain region.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ankush k. Singal whose telephone number is 5712701204. The examiner can normally be reached on monday-friday 7am-5pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, MATTHEW SMITH can be reached on (571)272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Khiem D. Nguyen/
Examiner, Art Unit 2823

/Ankush Singal/